

What Is Claimed Is:

1. A synchronization correction circuit comprising:
synchronization signal generating section for
successively receiving packets generated in accordance with a
5 designated cycle, from an external source, and generating a
packet synchronization signal in synchronization with the
reception cycle of these packets; and

interface control section for generating a transfer
clock for each respective data element contained in said
10 packets, on the basis of an internal clock, and making the
cycle of said transfer clock corresponding to the last data
element of said packet longer than the transfer clocks
corresponding to the other data elements, if the actual cycle
of said packet synchronization signal is longer than said
15 designated cycle, and making the cycle of said transfer clock
corresponding to the last data element of said packet shorter
than the transfer clocks corresponding to the other data
elements, if the actual cycle of said packet synchronization
signal is shorter than said designated cycle.

20 2. The synchronization correction circuit according to
claim 1, wherein said interface control section comprises:

a transmission interval counter for counting the
clock number of a measurement clock and resetting the count
value in accordance with said packet synchronization signal;

25 a detector for comparing the count result of said
transmission interval counter with a comparison value
specified in accordance with said designated cycle, and

outputting a detection signal if this count result matches the comparison value; and

a transfer clock generating section for resetting said transfer clock generation operation at the timing that said packet synchronization signal is input, and fixing the signal level of said transfer clock, when said detection signal is input.

3. The synchronization correction circuit according to claim 2, wherein said detector comprises:

10 a plurality of transmission interval comparators, for comparing the count result of said transmission interval counter with plural types of said comparison value corresponding respectively to plural types of said designated cycle;

15 and a type selector for selecting the output signal of the first transmission interval comparator corresponding to the designated cycle actually selected, from the output signals of said plurality of transmission interval comparators, and outputting a signal as a signal detection
20 signal.

4. The synchronization correction circuit according to claim 2, wherein said detector comprises:

a transmission interval comparator for comparing the count result of said transmission interval counter with said comparison value specified according to a common multiple of said plural types of designated cycle, and outputting a
25 signal as said detection signal.

5. The synchronization correction circuit according to claim 2, wherein said detector comprises:

a comparison value register for storing said comparison value;

5 a transmission interval comparator for comparing the count result of said transmission interval counter with said comparison value stored in said comparison value register;

10 a comparison stage number counter for counting the number of times that the count result of said transmission interval counter has reached said comparison value stored in said comparison value register;

a comparison stage number register for storing a comparison stage number; and

15 a stage number comparator for comparing the count result of said comparison stage number counter with said comparison stage number, and outputting the comparison result as said detection signal.

20 6. The synchronization correction circuit according to claim 5, wherein said stage number comparator outputs said comparison result as an interrupt signal to a central processing unit.

7. The synchronization correction circuit according to claim 5, wherein said detector comprises:

25 an average value storage section for storing the average cycle of said packet synchronization signal; and

a comparison value selector for selecting either
the value stored in the average value storage section or said
comparison value stored in said comparison value register,
and supplying said either value to said transmission interval
5 comparator.

8. The synchronization correction circuit according to
claim 2, further comprising transfer synchronization signal
generating section for generating a transfer synchronization
signal for achieving transfer synchronization of said packets
10 in word units, by using said transfer clock input from said
transfer clock generating section.